

PCT

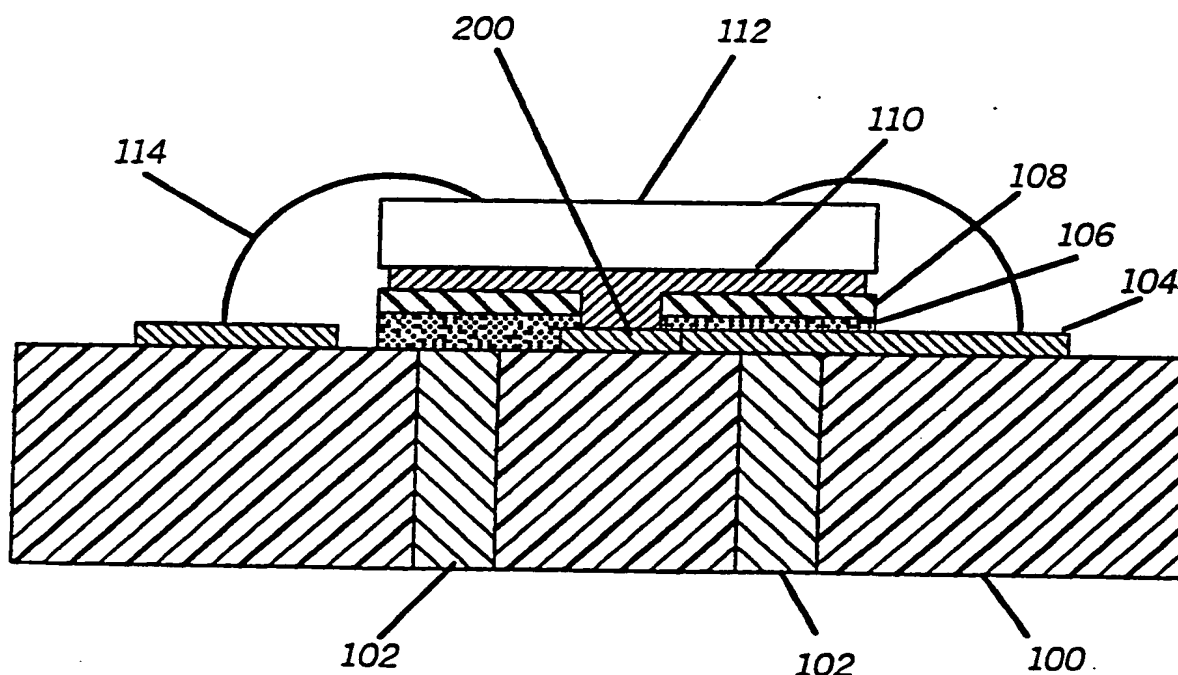
WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau



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(54) Title: METHOD OF GROUNDING AN ULTRA HIGH DENSITY PAD ARRAY CHIP CARRIER



(57) Abstract

A die pad (108) with a punched hole providing a throughway (110) is affixed upon the chip carrier base (100). Such throughway permits the electronic interconnection of the die backside (112) to a conductive runner (104) by means of electrically conductive material (110) set between the die backside (112) and the conductive runner (104).

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15     **METHOD OF GROUNDING AN ULTRA HIGH DENSITY  
PAD ARRAY CHIP CARRIER**

20     **Technical Field**

      This invention relates generally to a method of making an ultra high density pad array chip carrier, more particularly a method for grounding of an integrated circuit (I.C.) device in ultra high density pad array chip carriers.

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**Background Art**

      Grounding ultra high density chip carrier assemblies typically requires a wire bond from a conductive runner acting as ground on a substrate to a metallized polyimide film die pad. Wire  
30     bonding in chip carrier assemblies is disadvantageous due to the larger die pad size required to bond the wire, larger production and material costs, and lower current carrying capacities of typical bond wires such as a gold bond wire.

      Eliminating wire bonding to metallized polyimide film die  
35     pads reduces several undesirable effects. First, wire bonding requires a larger die pad to allow a wire bonder to place a wire

Figure 3 illustrates a top plan view of the chip carrier base with the die pad placed on top of the chip carrier base in accordance with the present invention.

**Detailed Description of the Preferred Embodiment**

- 5 Referring to Figure 1, there is shown an alumina ceramic substrate 100 having conductive areas (or metal runners) (104) deposited thereon. Some of these conductive areas terminate at a metal land (200) that serves as a common grounding point. Preferably, the metal land comprises a square having a size
- 10 dependent on the design of the substrate, although other shapes may be used. According to the invention, a convenient size of .020 inches X .020 inches (.051cm X .051cm) facilitates assembly. The metal land 200 is positioned directly below the through-hole in the die pad (108) shown in Figure 2.
- 15 Referring to Figure 2, the die pad (108) is affixed to at least a portion of the conductive areas (104) by means of an effective amount of adhesive, preferably Pyralux acrylic adhesive (106) made by Dupont. The die pad (108), either metallized or unmetallized, comprises of a polyimide film .002 inches (.005cm)
- 20 thick, and laminated with .001 inch (.003cm) Dupont Pyralux modified acrylic adhesive (106). Before the die pad is tacked onto the substrate, a hole, (preferably .020 inches (.051cm) to .100 inches (.255cm) in diameter) is formed in the polyimide film die pad and the attached Pyralux acrylic adhesive. This hole is
- 25 positioned in the die pad (106) so as to mount over the grounded metal land (200) on the ceramic substrate (100). Optimally, the solder filled throughholes (102) may be electronically connected to the conductive areas of the substrate (104) as is known in the art.
- 30 Referring to figures 2 and 3, the die pad and acrylic adhesive is then positioned on the substrate, which is then laminated. The lamination process causes an intimate bond between the die pad (108), the acrylic adhesive (106) and the conductive areas (104).
- 35 Preferably, a conductive material (110) comprising silver filled epoxy flows through the through-hole formed in the die pad

**Claims**

- 5           1.     A chip carrier assembly comprising:  
              a semiconductor chip;  
              a substrate including at least one conductive area;  
              a nonconductive die pad carried by the substrate  
              having at least one passage therethrough, and being positioned  
10           between the semiconductor and the substrate; and  
              an electrically conductive material, located in said  
              passage and between the substrate and the semiconductor chip  
              for providing electrical interconnection between the  
              semiconductor chip and said one conductive area of the  
15           substrate.

3. A chip carrier assembly comprising:
- a semiconductor chip;
  - a substrate including at least one conductive area;
  - a polyimide film die pad carried by the substrate
- 5 having at least one passage therethrough, and being positioned between the semiconductor and the substrate; and
- an electrically conductive material, located in said passage and between the substrate and the semiconductor chip for providing electrical interconnection between the
- 10 semiconductor chip and said one conductive area of the substrate.

6. A chip carrier assembly comprising:  
a semiconductor chip;  
an alumina ceramic substrate including conductive  
areas;  
5 a polyimide film die pad carried by the substrate  
having at least one passage therethrough, and being positioned  
between the semiconductor and the substrate, and  
an electrically conductive silver filled epoxy, located  
in said passage and between the substrate and the  
10 semiconductor chip for providing electrical interconnection  
between the semiconductor chip and said one conductive  
area of the substrate.

8. A chip carrier assembly for mounting a semiconductor chip comprising:
- 5 a semiconductor die;
  - a chip carrier base including metallic runners;
  - a polyimide film die pad with at least one pathway carried by the chip carrier base and positioned between the semiconductor die and said carrier base;
  - 10 electrically conductive material interconnecting said semiconductor die and at least one of said metallic runners through said pathway in said die pad.

12. A method for constructing a chip carrier assembly, comprising the steps of:

- (a) preparing a ceramic base;
- (b) laminating the die pad with an acrylic adhesive  
5 at a temperature so that the adhesive attaches to the die pad but does not begin to cure and punching a hole through said die pad and attached acrylic adhesive;
- (c) tacking said die pad onto a preheated ceramic base, positioning said punched hole in the die pad directly over a  
10 grounded conductive runner, forming a die pad bonded assembly;
- (d) heat laminating said die pad bonded assembly to fully cure the acrylic adhesive;
- (e) dispensing silver filled epoxy onto the  
15 middle of said die pad, forcing said silver filled epoxy through the said passway in the die pad so as to form an electronic connection between the die, which is placed into the epoxy, and said conductive runners.
- (f) placing the die onto the silver filled epoxy,  
20 thereby forming an electronic connection between the backside of the die and the conductive runners.



## AMENDED CLAIMS

[received by the International Bureau on 10 October 1990 (10.10.90);  
original claims 1, 3, 7, 8 and 11 amended ; other claims unchanged (5 pages)]

1. A chip carrier assembly comprising:
  - 5           a semiconductor chip, having a bottom surface;  
          a substrate including at least one conductive area;  
          a nonconductive die pad intimately bonded to at least  
one of the conductive areas of the substrate having at least one  
passage therethrough, and being positioned between the  
10 semiconductor chip and the substrate; and  
          an electrically conductive material, located in said  
passage and between the substrate and the semiconductor chip, for  
providing electrical interconnection between the semiconductor chip  
bottom surface and said one conductive area of the substrate.

7. A chip carrier assembly for mounting a semiconductor chip comprising:

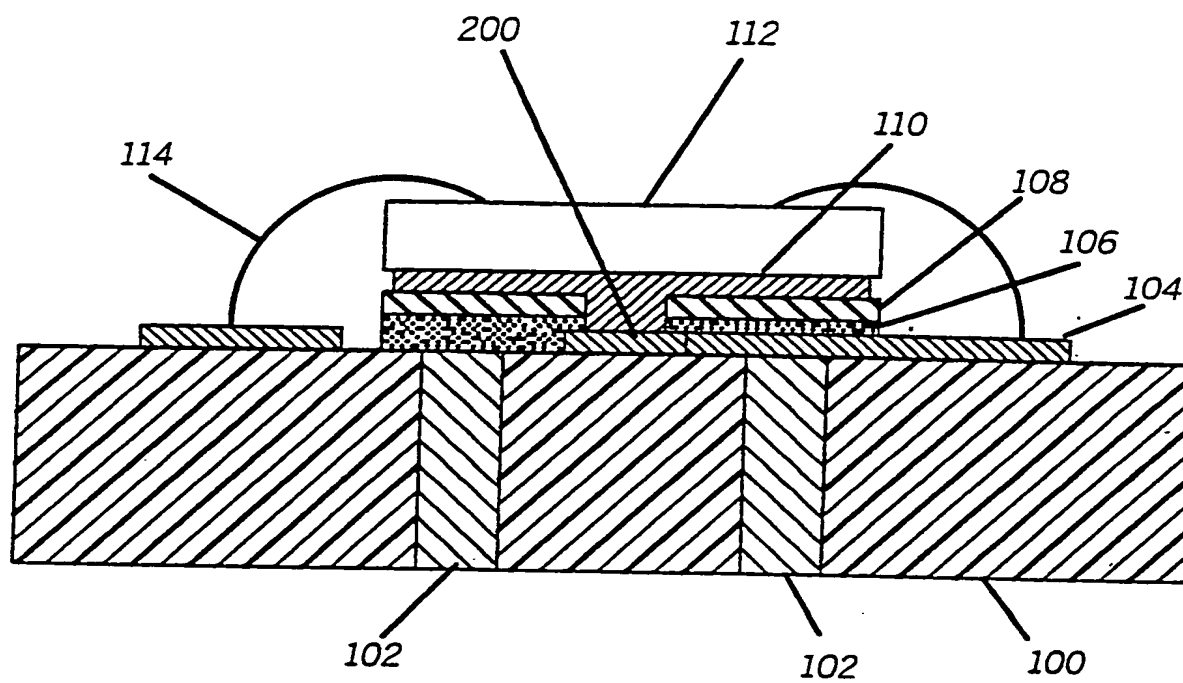
- 5           a semiconductor die, having a bottom surface;
- a chip carrier base including metallic runners;
- a nonconductive die pad with at least one pathway  
intimately bonded to at least one of the metallic runners on the chip  
carrier base and positioned between the semiconductor die and said  
carrier base;
- 10           electrically conductive material interconnecting said  
semiconductor die bottom surface and at least one of said metallic  
runners through said pathway in said die pad.

9. The chip carrier assembly of claim 7, wherein said chip carrier base comprises ceramic alumina.

10. The chip carrier assembly of claim 7, wherein said  
5 electrically conductive material comprises silver filled epoxy.

11. The chip carrier assembly of claim 7, wherein said pathway comprises a punched hole therethrough said die pad positioned directly above said metallic runner.

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*FIG. 2*

# INTERNATIONAL SEARCH REPORT

International Application No. PCT/US90/01828

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) \*

According to International Patent Classification (IPC) or to both National Classification and IPC  
 IPC(5): H05K 3/30 H01B 17/00 H01L 39/02 H05K 7/02: H05K 7/10  
 U.S. CL.: 29/832 174/138G 357/80 361/400,403

## II. FIELDS SEARCHED

Minimum Documentation Searched 7	
Classification System	Classification Symbols
U.S.	174/138G, 255,260 357/80 29/832 361/397, 400, 402, 403, 405, 406, 410, 414

Documentation Searched other than Minimum Documentation  
 to the Extent that such Documents are Included in the Fields Searched \*

## III. DOCUMENTS CONSIDERED TO BE RELEVANT \*

Category *	Citation of Document, 11 with indication, where appropriate, of the relevant passages 12	Relevant to Claim No. 13
X Y	US, A, 4,631,639 (BIRAUD) 23 December 1986, See entire document.	1, 7 1-3,6,8-9
A	US, A, 4,574,879 (DeGREE ET. AL.) 11 March 1986, See entire document.	

\* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

## IV. CERTIFICATION

Date of the Actual Completion of the International Search

17 JULY 1990

Date of Mailing of this International Search Report

14 AUG 1990

International Searching Authority

ISA/US

Signature of Authorized Officer

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INTERNATIONAL DIVISION